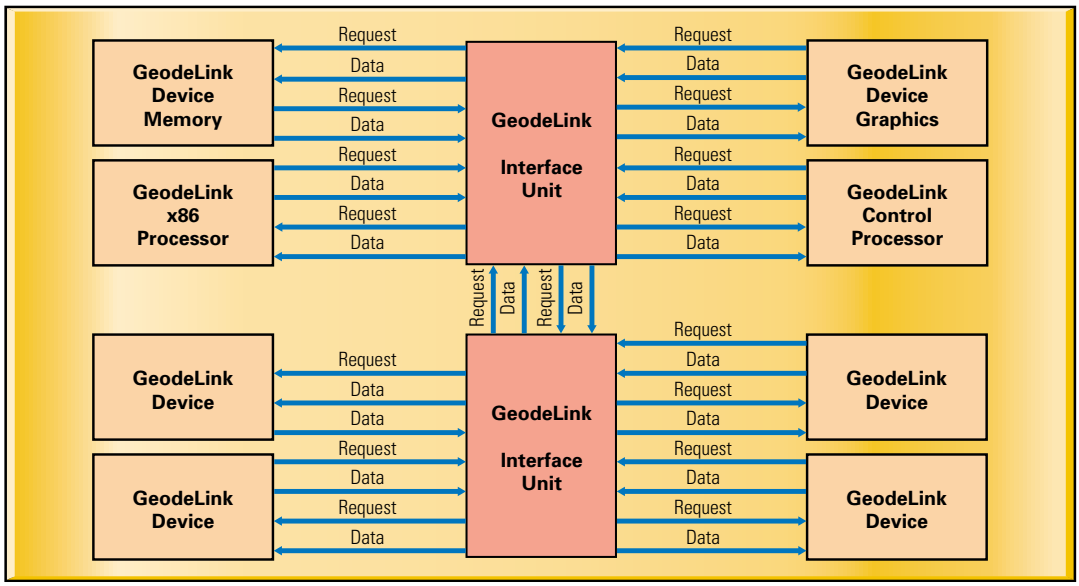
GeodeLink™ Architecture

A National Semiconductor Technology



GeodeLink System Architecture

GeodeLink™ Architecture

National Semiconductor announces its top to bottom system architecture for information appliance system-on-a chip. It is the first of its kind specifically designed for the Information Appliance space. The unique GeodeLink architecture offers a single on-chip interconnect that facilitates the integration of modules and allows the use of Unified Memory Architecture (UMA).

Unified Memory Architecture (UMA)

At the heart of the GeodeLink architecture is the built-in arbiter. The arbiter enables dynamic allocation of memory bandwith, with "on-the-fly" prioratization. Use of out of order data streams coupled with a high performance peer-to-peer communication enables direct communication between module, resulting in more efficient use of shared memory.

On-Chip Switched Fabric

At the core of the GeodeLink architecture lays a very high bandwith interface unit that can handle up to 6 GB/s of data transfer. With up to 31 pipelined transactions, the architecture increases the level of performance by allowing devices to have multiple simultaneous outstanding requests. This single bus architecture improves performance and facilitates IP reusability, thus improving our customer's time to market.

Advanced Hardware Power Management (AHPM)

The GeodeLink architecture has embedded power management features. This allows our OEM and ODM customers to take advantage of advanced power management without writing a single line of code. It is also OS independent, since the power management calls are handled at the BIOS level.

Development Software

The GeodeLink architecture has an embedded Enhanced JTAG interface that provides a consistent debug environment. With full bus master access and branch trace messaging capabilities, software development can be significantly accelerated.

GeodeLink

Technology Overview

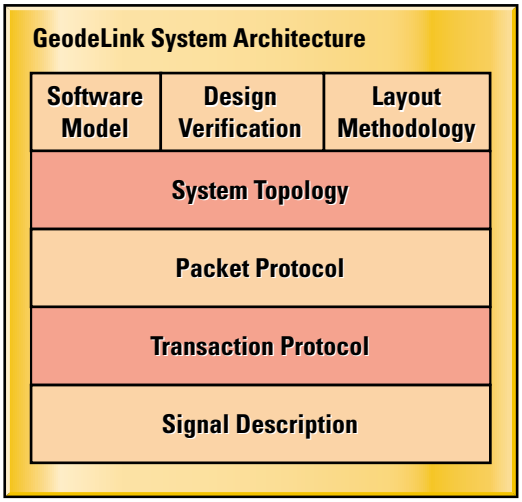
GeodeLink™ architecture is the first of its kind specifically designed for the IA space. Characteristics of the architecture include:

- **High performance on-chip switched fabric**
- **Optimized Unified Memory Architecture (UMA)**
- **Active Hardware Power Management (AHPM)**
- **Standard software model**
- **On-chip development support**

National Semiconductor

The Sight & Sound of Information

Technical Specifications



Architecture Characteristics:

- Standard bus interface for modular reusable IP
- Support for prioritization of accesses from real-time and isochronous devices
- Pipelining of multiple read and/or write requests from various devices (up to 31 pipelined Transactions)
- Extensible to a variety of bus widths (from 16 to 256 bits) and clock rates (33-300 MHz)
- Standard bridges to legacy buses (XBus, PCI)
- Peer to Peer communication
- Active Hardware Power Management (AHPM)
- Suspend clocks and power controls
- Standard test and scan interface
- Standard diagnostic signals
- On chip logic analyzer functions
- Full Scan for debug
- Error reporting for debug
- GeodeLink virtual PCI headers

Operating Systems

National Semiconductor will support the following operating systems for all of its devices using the Geode architecture:

- Windows® CE 3.0 and 4.0
- Linux® (Kernel 2.4)
- Windows NT® and NTe
- Windows XP and XPe

Other Operating Systems

Any x86 compatible operating system can be used with the GeodeLink architecture by developing the appropriate device drivers. Contact National Semiconductor for availability.

Availability

National Semiconductor will release its first samples based on the GeodeLink architecture in Q3'01, with production slated for H1'02. All future IA devices at National Semiconductor will use this architecture.

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052
1 408 721 5000

Visit our web site at:
national.com/geodelink

For more information, send email to:
geode@nsc.com

National Semiconductor
The Sight & Sound of Information